

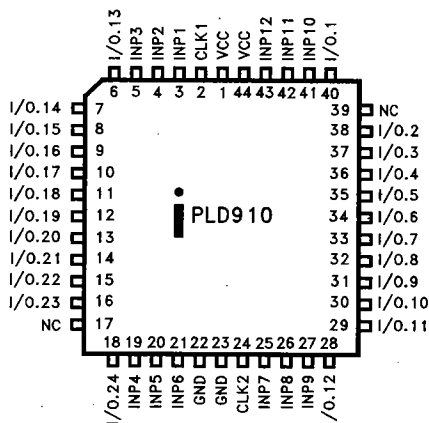
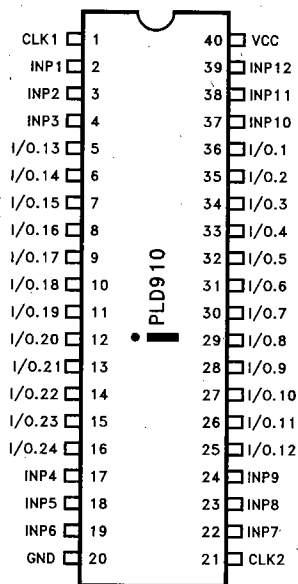


iPLD910/85C090 FAST 24-MACROCELL CMOS PLD

**Function, Pin, and JEDEC Compatible with
EP900, EP910, EP910A, 85C090 and 5C090**

- t_{PD} 12 ns, 62.5 MHz w/Feedback, Clock to Output 8 ns
- $I_{CC} = 150$ mA Max @ 1 MHz
- 24 Macrocells with Programmable I/O Architecture (Register/Combinatorial). Registers Configurable as D/T/JK/RS Types
- Up to 36 Inputs (12 Dedicated and 24 I/O)
- 8 P-terms, Selectable SOP Invert, Clear and OE P-terms for Each Macrocell
- Programmable Clock System with 2 Synchronous Clocks and Asynchronous Clocking Option on all Macrocells
- Extensive Software and Programming Support via Intel and Third-Party Tools
- 1-Micron CHMOS IIIE* EPROM Technology
- Programmable Low-Power Option for "Standby" Operation; 60 μ A Typ. in Standby Mode
- Programmable Security Bit Allows Total Protection of Proprietary Designs
- 100% Generically Tested Logic Array
- Available in 40-Pin PDIP and 44-Pin PLCC Packages
- 85C090 also Available in 40-pin CerDIP Package

(See Packaging Spec., Order Number 240800-001, Package Type N and P)



290456-1

Figure 1. Pinout Diagrams

*CHMOS is a patented process of Intel Corporation.

85C090

All information in this document that refers to the iPLD910 is identical to that of the 85C090.

INTRODUCTION

The iPLD910 is a high-performance, high-integration, general-purpose CMOS PLD. The iPLD910 PLD

(Programmable Logic Device) accommodates logic functions with up to 36 inputs and 24 I/O macrocells. Each I/O macrocell includes 8 product-terms (p-terms) for input, a separate clear p-term, and an output enable/asynchronous clock p-term. With a maximum external frequency of 62.5 MHz, the iPLD910 is well suited to high-performance micro-processor-based systems. The iPLD910 is pin- and function-compatible with the EP900, EP910, EP910A, 85090 and 5C090.

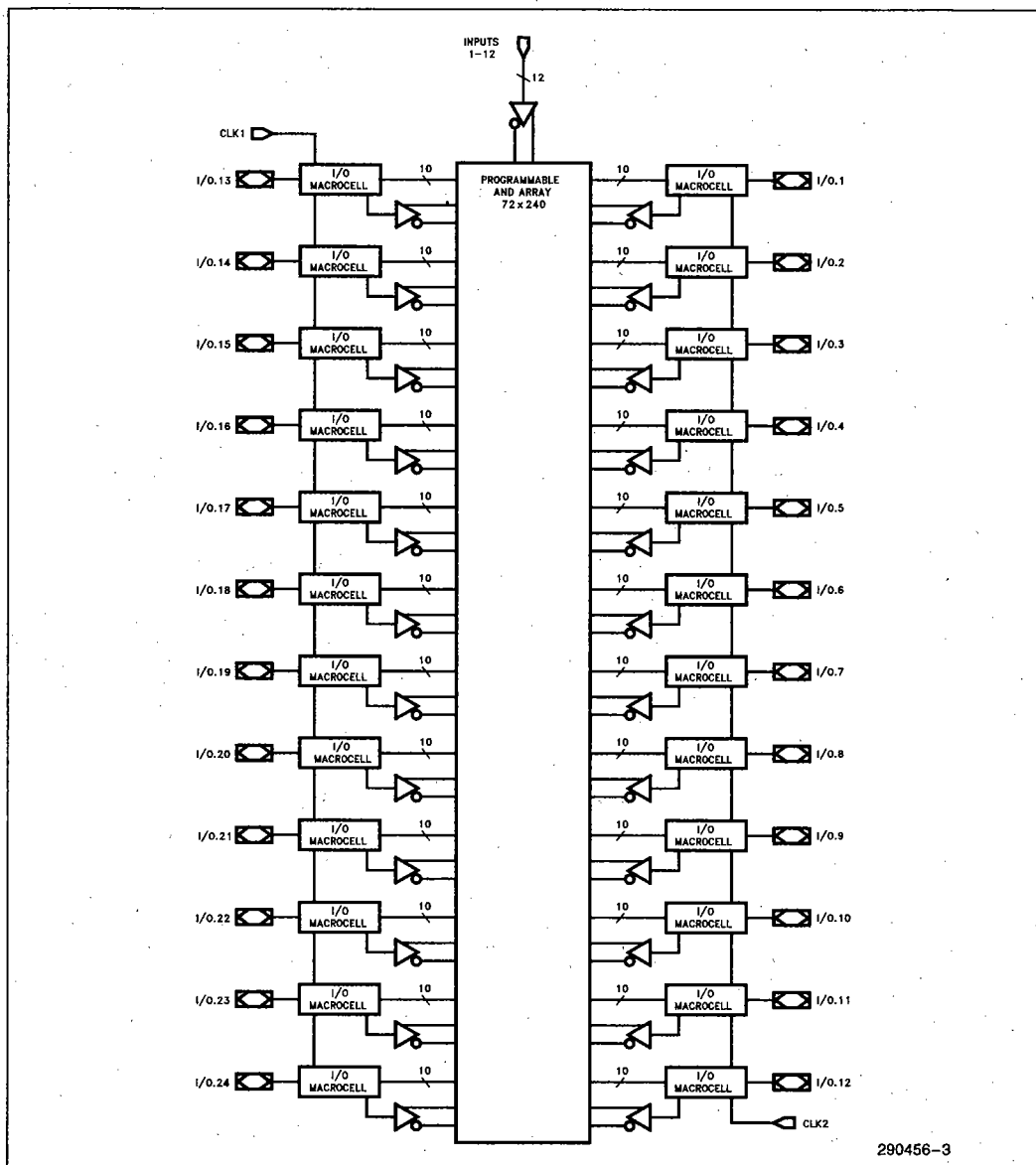


Figure 2. iPLD910 Global Architecture

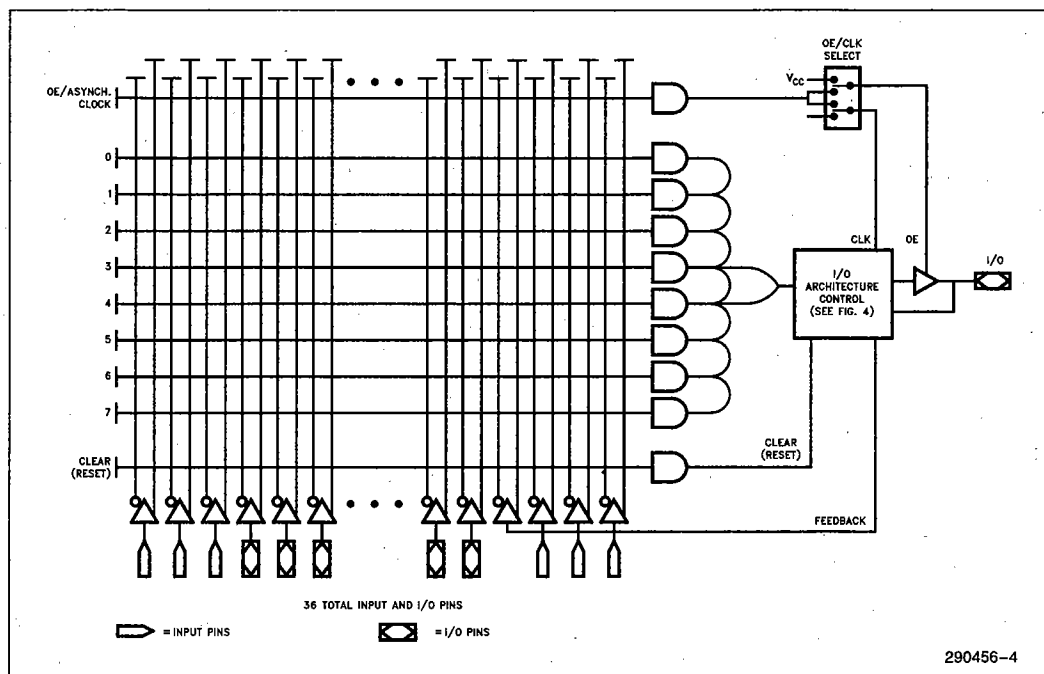


Figure 3. iPLD910 Macrocell Architecture

The iPLD910 uses CHMOS EPROM (floating gate) cells as logic control elements instead of fuses. The CHMOS EPROM technology reduces power consumption without sacrificing speed. In addition, Intel's advanced CHMOS III-E EPROM process technology enables higher logic densities to be achieved with superior speed and low-power performance over other comparable devices. Intel's μ PLDs add the benefits of "zero" stand-by power not available on other programmable logic devices. EPROM technology allows these devices to be 100% factory tested by programming and erasing all the EPROM logic control elements.

The architecture of the iPLD910 is based on the "Sum of Products" PLA (Programmable Logic Array) structure with a programmable AND array feeding into a fixed OR array. The device accommodates combinational and sequential logic functions. A programmable I/O architecture provides individual selection of either combinatorial or registered output and feedback signals all with selectable polarity.

A feature unique to the iPLD910 is the ability to individually program the output registers as a D-, T-, SR-, or JK-type Flip-Flop without sacrificing the utilization of programmable AND logic. Each output register can be individually clocked from any of the input or feedback paths available within the AND array. With these features, a wide variety of logic

functions can be simultaneously implemented—all on the same device.

ARCHITECTURE DESCRIPTION

The iPLD910 has 12 dedicated inputs, 24 I/O pins that may be configured for input, output, or bidirectional operations, and 2 synchronous clock inputs. The iPLD910 is packaged in a 40-lead windowed ceramic DIP or OTP plastic or 44-lead OTP J-leaded chip carrier package.

The basic Macrocell architecture for the iPLD910 is shown in Figure 3. The iPLD910 has 24 of these macrocells (one for each I/O pin). The Macrocell is organized in the familiar sum-of-products structure with a programmable AND array attached to a fixed OR term. The inputs to the programmable AND array originate from the true and complement signals from each of the dedicated input pins and each of the I/O control blocks.

The AND array for the iPLD910 has 72 inputs derived from the true and complement signals at the input and I/O pins. The AND array in the iPLD910 encompasses 240 product terms which are distributed among the 24 Macrocells. The global device architecture is shown in Figure 2.

Each Macrocell contains ten product terms. Eight of the ten product terms (AND gates) are dedicated for SOP logic implementation. One product term on each Macrocell is used for RESET control to the output register associated with the Macrocell. The final product term is used for OE/Asynchronous Clock implementation.

Within the AND array, there is an EPROM connection at every intersection of an input signal (true and complement) and a product term to a given Macrocell. Before programming an erased device, every EPROM connection is made at every intersection. But during the programming process, these connections are opened so that only the desired connections remain. Therefore, the true or complement of any input signal can be connected to any product term. If both the true and complement connections of any signal are left intact, a logical false results on the output of the AND gate. However, if both the true and complement connections are open, then a logic "don't care" results on the AND gate. Lastly, if all the inputs of a product term are programmed open, then a logical true results on the output of the AND gate.

The iPLD910 has two dedicated clock inputs to provide synchronous clock signals to the internal registers. Each of the clock signals controls half the total registers within the given device. For example, CLK1 provides synchronous clocking to the registers in Macrocells in the left half of the array while CLK2 controls the registers associated with Macrocells in the right half of the array. The advanced I/O architecture allows for any number of the registers to be synchronously clocked (from none to all). Both of the dedicated clock inputs latch the data into a given register when triggered on a positive edge.

MACROCELL ARCHITECTURE SELECTION

The iPLD910 architecture provides each Macrocell with over 50 different possible I/O register configurations. Each I/O pin can be configured for combinatorial or registered output (true or complement) with feedback. In addition, four different types of output registers can be implemented on I/O pin without any additional logic requirements. The feedback mechanism for each register back into the AND array can be programmed to provide for either registered feedback from the Macrocell or input feedback (treating the pin as an input). Another advantage of the advanced I/O capability of the iPLD910 is the ability to individually clock each internal register from asynchronous clock signals.

Invert Select EPROM Bit

The Invert Select EPROM bit is used to invert the product term input into the register. This applies to all inputs including double inputs on the JK and SR registers.

REGISTER SELECTION

The advanced I/O architecture of the iPLD910 allows four different register types along with combinatorial output as illustrated in Figure 4a through e. The register types include a T, D, JK, or SR Flip-Flop and each Macrocell I/O structure may be independently configured. In addition, all registers have an individual asynchronous RESET control from a dedicated product term derived in the AND array. When this dedicated product term is a logical one, the Macrocell register is immediately cleared to a logical zero independent of the register clock. The RESET function occurs automatically on power-up.

2

Output Register Configuration

The four different register types shown in Figure 4 are described below.

D- or T-type Flip-Flops

When either a D- or T-type Flip-Flop is configured as part of the I/O structure, all eight of the product terms into the Macrocell are ORed together and fed into the register input.

JK or SR Registers

When either a JK or SR register is configured, the eight product terms are shared among two OR gates (one for the J or S input and the other for the K or R input). The allocation for these product terms for each of the register inputs is optimized by the PLDshell Plus software.

OUTPUT/FEEDBACK

The Output Select Multiplexer allows for either registered, combinatorial or no output.

The Feedback Select Multiplexer EPROM bit enables registered, I/O (using the pin for bidirectional input or just input), or no feedback to the AND array.

The Feedback Select is also important for building equations with more than 8 product terms. The 8-product equations of a Macrocell can be fed back

into the AND array and combined with still more signals to create a much larger product term (of more than 8-inputs). If the feedback product term is not to be used as an output, the associated Macrocell pin should be left floating (no connect) when assembled onto a circuit board.

Any I/O pin may be configured as a dedicated input by selecting no output and pin feedback through the appropriate multiplexers.

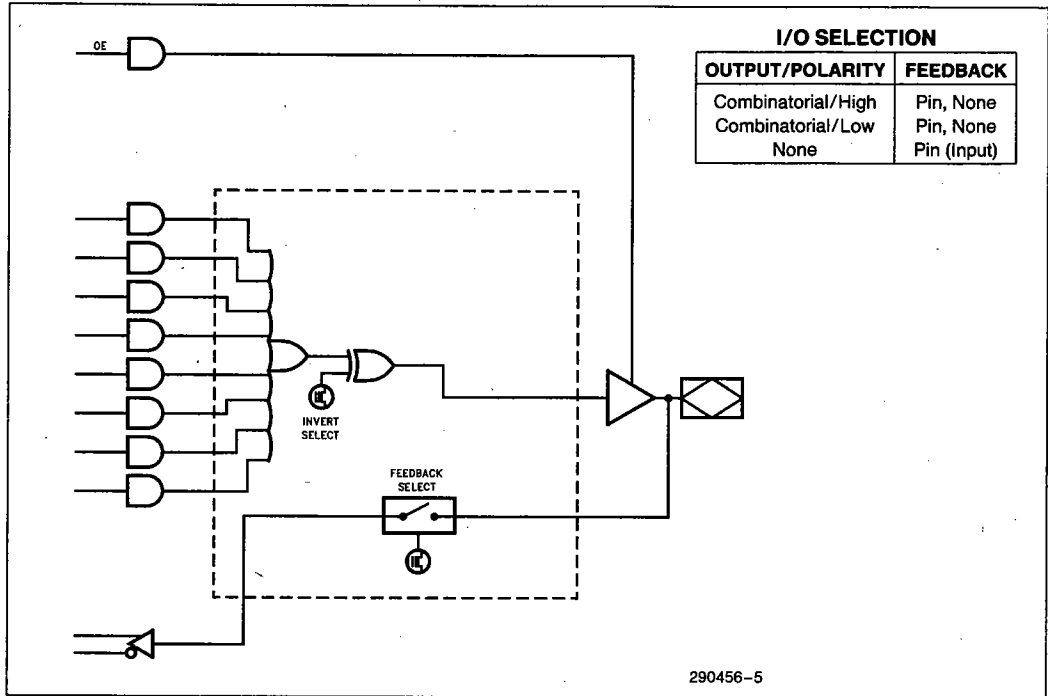


Figure 4a. Combinatorial I/O Configuration

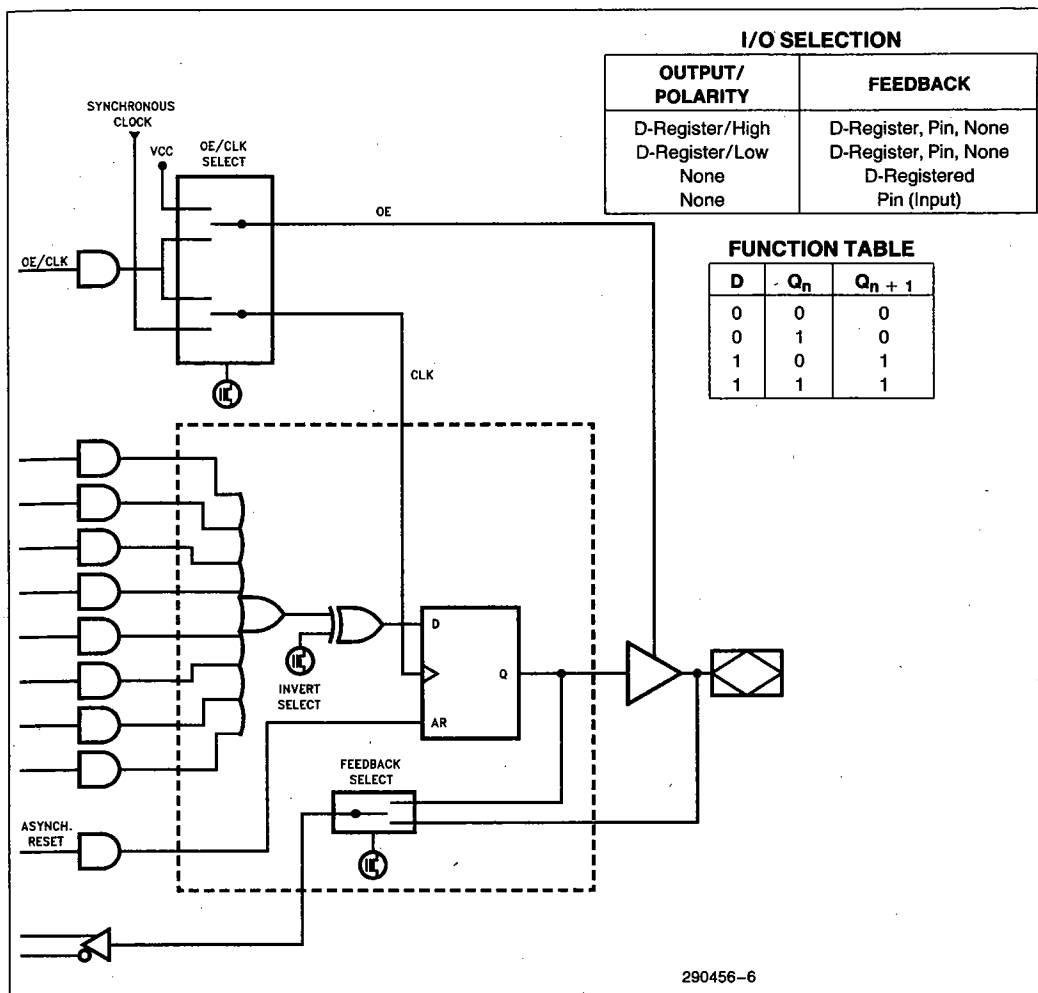


Figure 4b. D-Type Flip-Flop Register Configuration

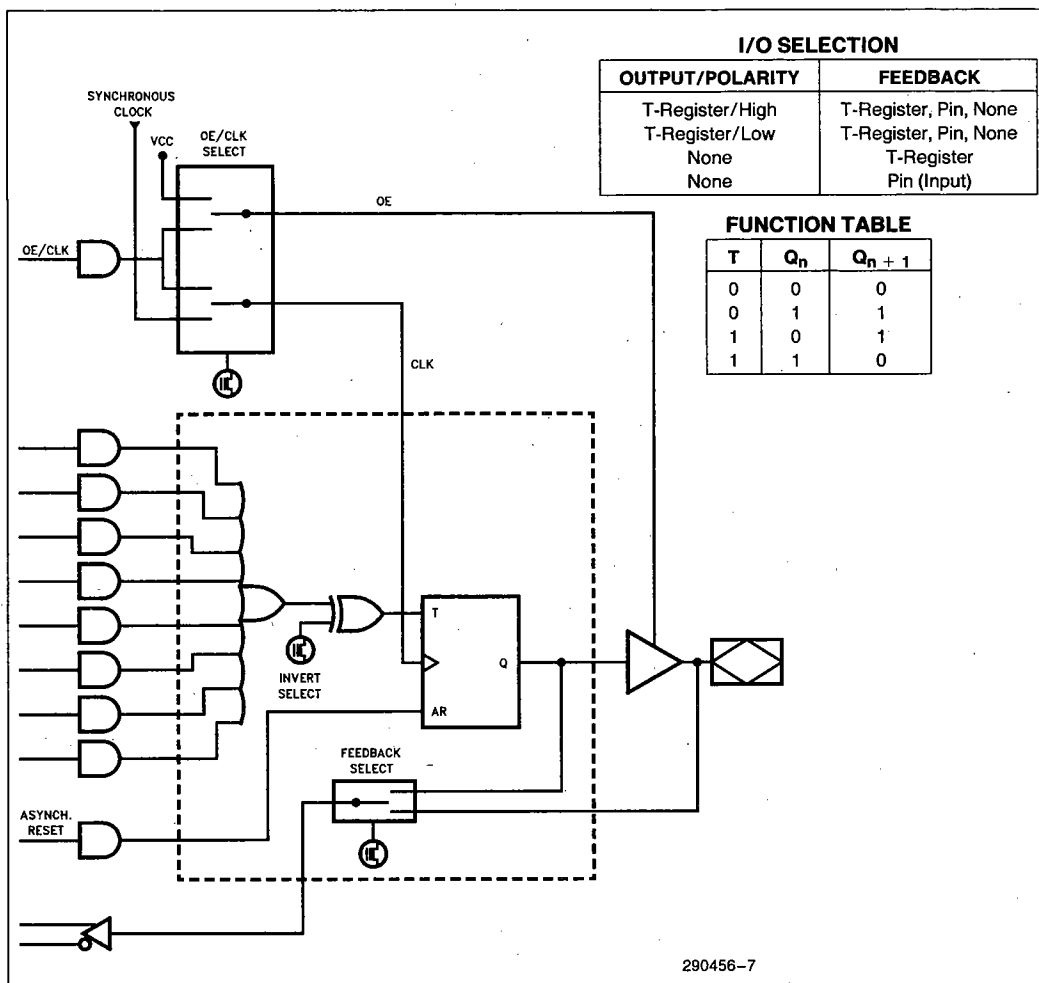


Figure 4c. Toggle Flip-Flop Register Configuration

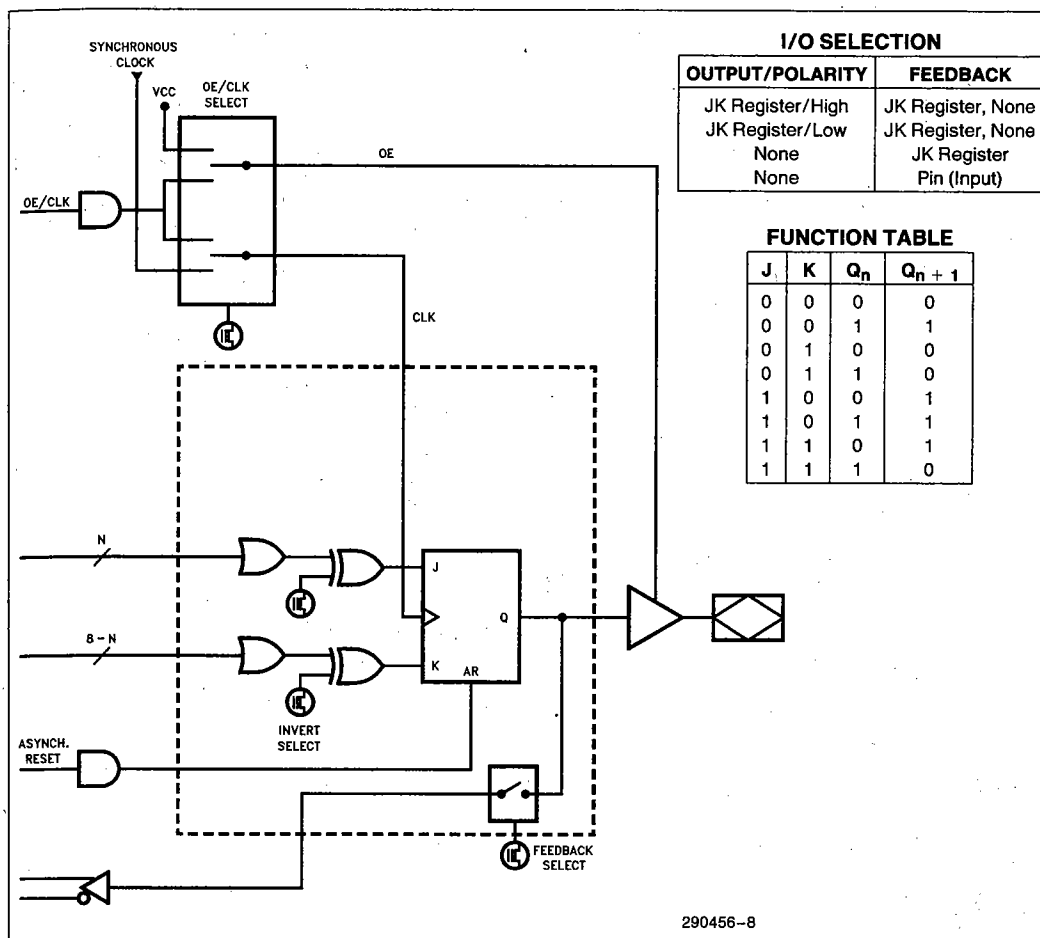


Figure 4d. JK Flip-Flop Register Configuration

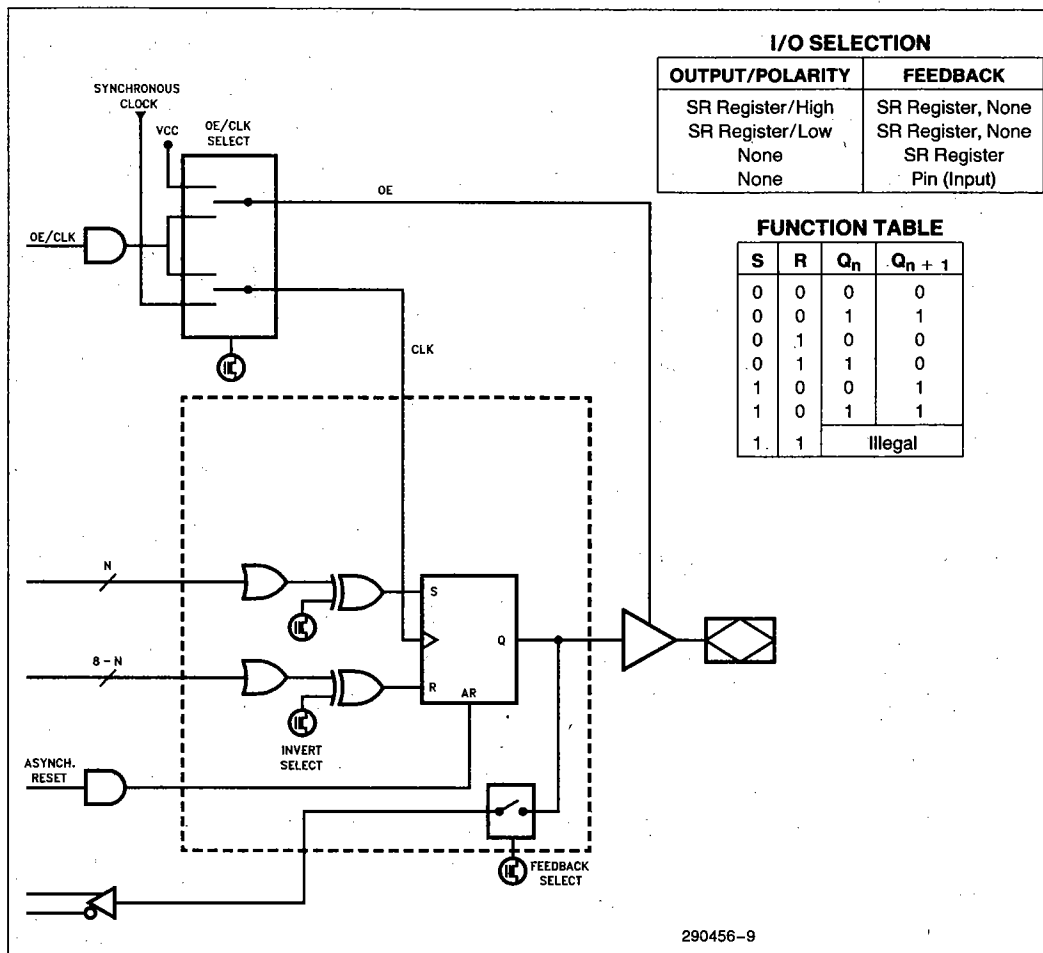


Figure 4e. SR Flip-Flop Register Configuration

Output Enable (OE)/Clock Selection

Two modes of operation are provided by the OE/CLK Select Multiplexer as a part of each Macrocell. One mode provides for three-state buffering of outputs while in the other mode, the outputs are always enabled. The operation of the OE/CLK Select Multiplexer sets the mode within a given Macrocell. Therefore, the output mode can be selected individually on every output. Figure 5 illustrates the two modes of OE/CLK operation.

MODE 0: THREE-STATE BUFFERING

In Mode 0, the three-state output buffer is controlled by a single product term originating from the AND array. The output is enabled when the product term is a logical true. Conversely, the output appears as high impedance when the product term is a logical false as shown in Table 1. In Mode 0, the Macrocell Flip-Flop is connected to its associated synchronous clock (either CLK1 or CLK2 depending upon the Macrocell's location within the device). Thus, the Macrocell Flip-Flop may be clocked by its respective synchronous clock but its output will not become valid until the output is enabled.

Table 1. Mode 0 Output Selection

Product Term	Output Buffer
FALSE	Three-State
TRUE	Enabled

MODE 1: OUTPUT BUFFER ENABLED

In Mode 1, the Output Buffer is always enabled. In addition, the Macrocell Flip-Flop is connected to the AND array. The Macrocell Flip-Flop may now be triggered from an asynchronous clock signal generated by the AND array logic to the OE/CLK multiplexable term. Mode 1 allows the Macrocell Flip-Flops to be individually clocked from any of the available signals in the AND array. Since both true and complement values appear in the AND array, the Flip-Flop may be clocked by positive-or negative-going signals at any input pin. Gated clock structures can be created since the Flip-Flop clock is created by a product term.

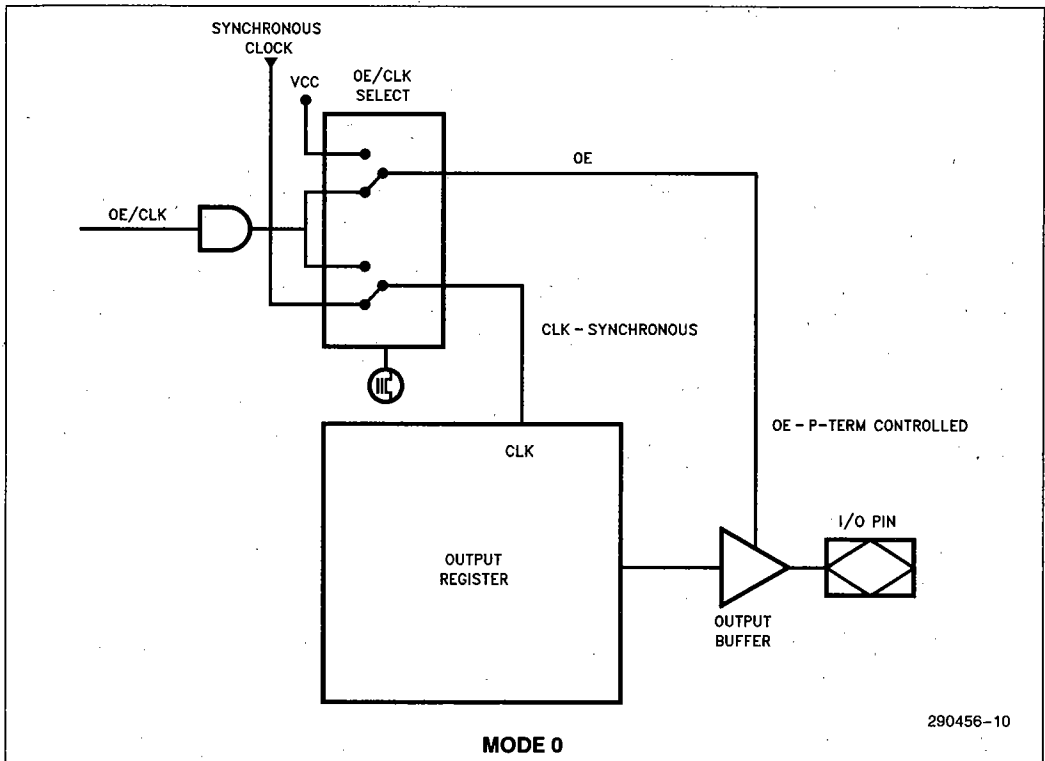


Figure 5. Output Enable/Clock Configuration

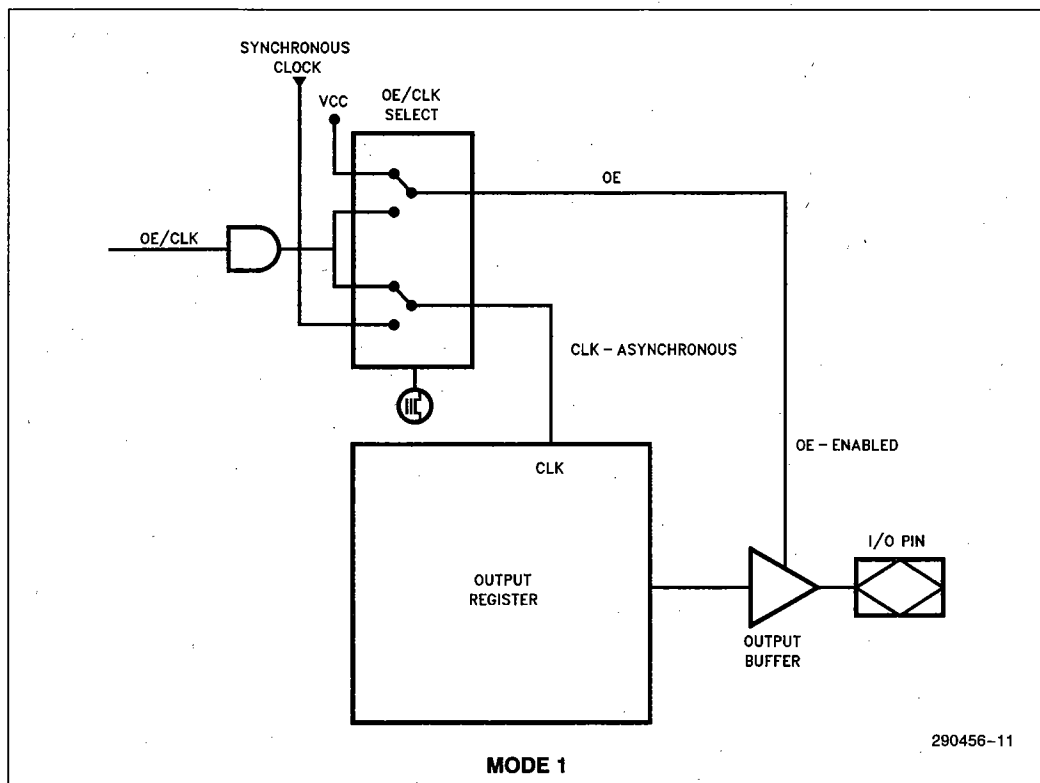


Figure 5. Output Enable/Clock Configuration (Continued)

AUTOMATIC STAND-BY MODE

The iPLD910 contains a programmable bit, the Turbo Bit, that optimizes operation for speed or for power savings. When the Turbo Bit is programmed (TURBO = ON), the device is optimized for maximum speed. When the Turbo Bit is not programmed (TURBO = OFF), the device is optimized for power savings by entering standby mode during periods of inactivity.

Figure 6 shows the device entering standby mode approximately 75 ns after the last input transition.

When the next input transition is detected, the device returns to active mode. Wakeup time adds an additional 40 ns to the propagation delay through the device as measured from the first input. No delay will occur if an output is dependent on more than one input and the last of the inputs changes after the device has returned to active mode.

After erasure, the Turbo Bit is unprogrammed (OFF); automatic standby mode is enabled. When the Turbo Bit is programmed (ON), the device never enters standby mode.

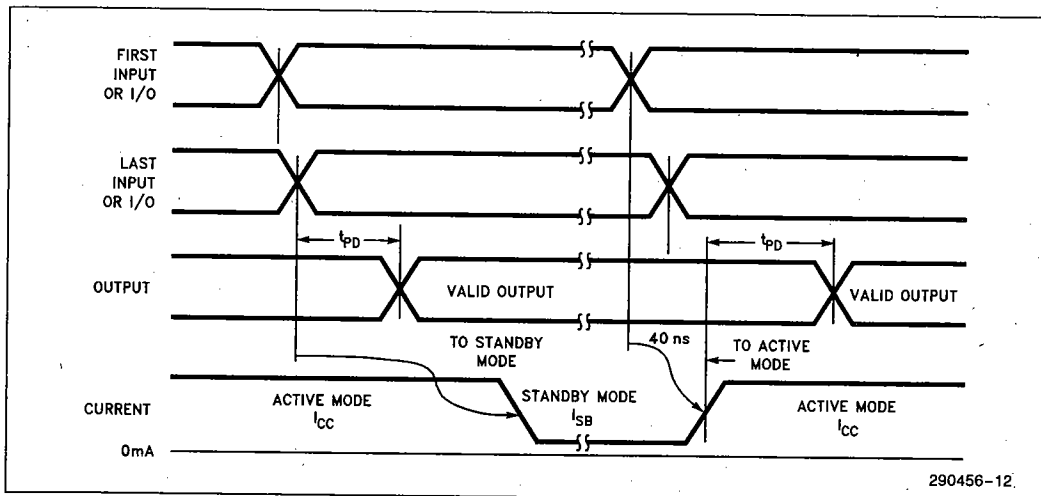


Figure 6. iPLD910 Standby and Active Mode Transitions

Erased-State Configuration

Prior to programming, the I/O structure is configured for combinatorial active low output with input (pin) feedback.

PROGRAMMING CHARACTERISTICS

Initially, all the EPROM control bits of the iPLD910 are connected (in the "1" state). Each of the connected control bits are selectively disconnected by programming the EPROM cells into their "0" state. Programming voltage and waveform specifications are available by request from Intel to support programming of the iPLD910.

Intelligent Programming Algorithm

The iPLD910 supports the Intelligent Programming Algorithm which rapidly programs Intel PLDs while ensuring programming reliability as the incremental program margin of each bit is continually monitored to determine when the bit has been successfully programmed.

FUNCTIONAL TESTING

Since the logical operation of the iPLD910 is controlled by EPROM elements, the device is completely testable. Each programmable EPROM bit controlling the internal logic is tested using application-independent test program patterns. After testing, the devices are erased before shipment to customers. No post-programming tests of the EPROM array are required.

The testability and reliability of EPROM-based programmable logic devices is an important feature over similar devices based on fuse technology. Fuse-based programmable logic devices require a user to perform post-programming tests to insure proper programming. These tests must be done at the device level because of the cumulative error effect. For example, a board containing ten devices each possessing a 2% device fallout translates into an 18% fallout at the board level (it should be noted that programming fallout of fuse-based programmable logic devices is typically 2% or higher).

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range $GND < (V_{IN} \text{ or } V_{OUT}) < V_{CC}$. Unused inputs and I/Os should be tied to V_{CC} or GND to minimize device power consumption. Reserved pins (as indicated in the logic compiler REPORT file) should be left floating (no connect) so that the pin can attain the appropriate logic level. A power supply decoupling capacitor of at least $0.2 \mu F$ must be connected directly between V_{CC} and GND pins of the device.

As with all CMOS devices, ESD handling procedures should be used with the iPLD910 to prevent damage to the device during programming, assembly and test.

DESIGN SECURITY

A single EPROM bit provides a programmable design security feature that controls the access to the data programmed into the device. If this bit is set, a proprietary design within the device cannot be copied. This EPROM security bit enables a higher degree of design security than fused-based devices since programmed data within EPROM cells is invisible even to microscopic evaluation. The EPROM security bit, along with all the other EPROM control bits, will be reset by erasing the device.

LATCH-UP IMMUNITY

All of the input, I/O, and clock pins of the iPLD910 have been designed to resist latch-up which is inherent in inferior CMOS structures. The iPLD910 is designed with Intel's proprietary CHMOS II-E EPROM process. Thus, each of the pins will not experience latch-up with currents up to ± 100 mA and voltages ranging from $-1V$ to $(V_{CC} + 1V)$. Furthermore, the programming pin is designed to resist latch-up to the 13.5V maximum device limit.

DEVELOPMENT SOFTWARE

Third Party Support

The PLD910 is also supported by third-party logic compilers such as ABEL*, CUPL*, PLDesigner*,

Log/IC, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

Full logic compilation and functional simulation for the iPLD910 is supported by PLDshell Plus software. The GUI Logic IID provides programming support on Intel programmers.

PLDshell Plus

PLDshell Plus design software is Intel's new, user-friendly design tool for PLD design. PLDshell Plus allows user's to incorporate their preferred text editor, programming software, and additional design tools into a easy-to-use, menued design environment that includes Intel's PLDasm™ logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, datasheet briefs, technical notes, and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative.

*ABEL is a trademark of Data I/O Corporation.

CUPL is a trademark of Logical Devices, Inc.

PLDesigner is a trademark of MINC, Inc.

Log/IC™ is a trademark of ISDATA, Corporation.

ADF PRIMITIVES SUPPORTED

The following ADF primitives are supported by this device:

INP	JOJF
CONF	JONF
COIF	SONF
RONF	SOSF
RORF	TOIF
ROIF	TONF
NORF	TOTF
NOJF	CLKB
NOSF	
NOTF	

ORDERING INFORMATION

f _{CNT1} (MHz)	f _{MAX} (MHz)	t _{PD} (ns)	Order Code	Package	Operating Range
62.5	100	12	P PLD910-12	PDIP	Commercial
			N PLD910-12	PLCC	Commercial
			D85C090-12	*CerDIP	Commercial
			P85C090-12	PDIP	Commercial
			N85C090-12	PLCC	Commercial
50	83.3	15	P PLD910-15	PDIP	Commercial
			N PLD910-15	PLCC	Commercial
			D85C090-15	*CerDIP	Commercial
			P85C090-15	PDIP	Commercial
			N85C090-15	PLCC	Commercial
33.3	50	25	P PLD910-25	PDIP	Commercial
			N PLD910-25	PLCC	Commercial
			D85C090-25	*CerDIP	Commercial
			P85C090-25	PDIP	Commercial
			N85C090-25	PLCC	Commercial
			TD85C090-25	*CerDIP	Industrial
			TN85C090-25	PLCC	Industrial

Commercial: 0°C to +70°C

Industrial: -40°C to +85°C

*Windowed package allows UV erase.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Units
V _{CC}	Supply Voltage ⁽¹⁾	-2.0	7.0	V
V _{pp}	Programming Supply Voltage ⁽¹⁾	-2.0	13.5	V
V _I	DC Input Voltage ⁽¹⁾⁽²⁾	-0.5	V _{CC} + 0.5	V
t _{stg}	Storage Temperature	-65	+150	°C
t _{amb}	Ambient Temperature ⁽³⁾	-10	+85	°C

NOTES:

1. Voltages with respect to ground.
2. Minimum DC input is -0.5V. During transitions, the inputs may undershoot to -2.0V or overshoot to +7.0V for periods less than 20 ns under no load conditions.
3. Under bias. Extended temperature versions are also available.

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	4.75	5.25	V
V _{IN}	Input Voltage	0	V _{CC}	V
V _O	Output Voltage	0	V _{CC}	V
T _A	Operating Temperature	0	+70	°C
t _R	Input Rise Time		500	ns
t _F	Input Fall Time		500	ns

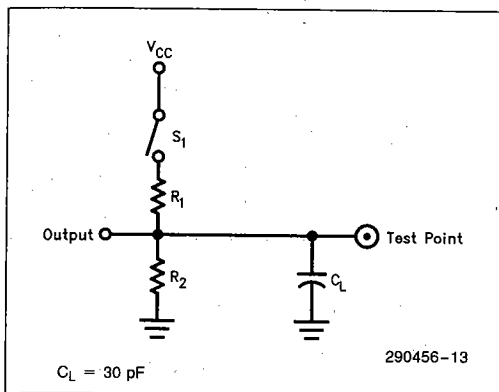
D.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IH} ⁽⁴⁾	High Level Input Voltage	2.0		V _{CC} + 0.3	V	
V _{IL} ⁽⁴⁾	Low Level Input Voltage	-0.3		0.8	V	
V _{OH}	High Level Output Voltage	2.4			V	I _O = -4.0 mA D.C., V _{CC} = min.
V _{OL} ⁽⁵⁾	Low Level Output Voltage			0.45	V	I _O = 12.0 mA D.C., V _{CC} = min.
I _I	Input Leakage Current	-10		+10	μA	V _{CC} = max., GND < V _{IN} < V _{CC}
I _{OZ}	Output Leakage Current	-10		+10	μA	V _{CC} = max., GND < V _{OUT} < V _{CC}
I _{SC} ⁽⁶⁾	Output Short Circuit Current	-30		-120	mA	V _{CC} = max., V _{OUT} = 0.5V
I _{SB} ⁽⁷⁾	Standby Current		60	150	μA	V _{CC} = max., V _{IN} = V _{CC} or GND, Standby Mode
I _{CC}	Power Supply Current (See I _{CC} vs. Freq. Graph)		4	12	mA	V _{CC} = max., V _{IN} = V _{CC} or GND, No Load, f _{IN} = 1 MHz, Device Prog. as Two 12-Bit Counters, Turbo = Off
			120	150	mA	Turbo = On, f _{IN} = 1 MHz
I _{CCI}	Power Supply Current Industrial Temperature			180	mA	Turbo = On, f _{IN} = 1 MHz

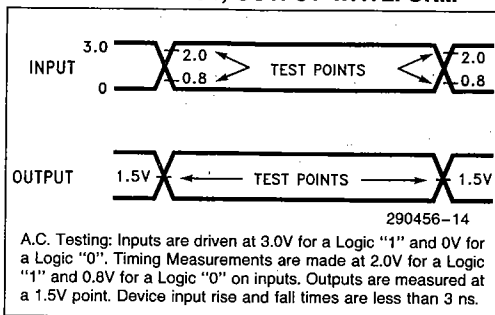
NOTES:

4. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
5. Maximum DC I_{OL} for the device is 96 mA for CLK1 group I/O.1-I/O.12 and 96 mA for CLK2 group I/O.13-I/O.24.
6. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.
7. In Non-Turbo Mode (TURBO = OFF), device enters standby mode approximately 75 ns after the last input transition.

A.C. TESTING LOAD CIRCUIT



A.C. TESTING INPUT, OUTPUT WAVEFORM



SWITCHING TEST CIRCUIT

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}	Closed	30 pF	200 Ω	330 Ω	1.5V
t_{PZX}	Z \rightarrow H: Open Z \rightarrow L: Closed				1.5V
t_{PXZ}	H \rightarrow Z: Open L \rightarrow Z: Closed	5 pF			H \rightarrow Z: $V_{OH} - 0.5V$ L \rightarrow Z: $V_{OL} + 0.5V$

CAPACITANCE $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{CC} = 5.0V \pm 5\%$ (8)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V, f = 1.0 \text{ MHz}$		5	8	pF
C_{IO}	I/O Capacitance	$V_{OUT} = 0V, f = 1.0 \text{ MHz}$		6	8	pF
C_{CLK}	CLK Capacitance	$V_{OUT} = 0V, f = 1.0 \text{ MHz}$		8	10	pF
C_{VPP}	V_{PP} Pin Capacitance	V_{PP} on CLK2, $f = 1.0 \text{ MHz}$		10	12	pF

NOTES:

8. These values are evaluated at initial characterization and whenever design modifications occur that may affect capacitance.

COMBINATORIAL MODE A.C. CHARACTERISTICS

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0V \pm 5\%$ (9)

Symbol	Parameter	iPLD910-12			iPLD910-15			iPLD910-25			Non-(10) Turbo Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
$t_{PD}^{(11)}$	Input or I/O to Output Valid w/ 8 Outputs Switching			12			15			25	+40	ns
$t_{PZX}^{(12)}$	Input or I/O to Output Enable			15			18			28	+40	ns

COMBINATORIAL MODE A.C. CHARACTERISTICS (Continued)

$T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$ (9)

Symbol	Parameter	iPLD910-12			iPLD910-15			iPLD910-25			Non-(10) Turbo Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
$t_{PXZ}^{(12)}$	Input or I/O to Output Disable			15			18			28	+ 40	ns
t_{CLR}	Input or I/O to Asynch. Reset			15			18			28	+ 40	ns

NOTES:

9. Typical values are at $T_A = 25^{\circ}\text{C}$, $V_{CC} = 5\text{V}$, Active Mode.

10. If device is operated in Non-Turbo Mode (TURBO = OFF) and the device is inactive for approx. 75 ns, increase time by amount shown.

11. Measured with eight outputs switching. See t_{PD} vs. Number of Outputs Switching graph.

12. t_{PZX} and t_{PXZ} are measured at $\pm 0.5\text{V}$ from steady state voltage as driven by spec. output load.

REGISTER MODE—SYNCHRONOUS CLOCK A.C. CHARACTERISTICS

$T_A = 0^{\circ}\text{C}$ to 70°C , $V_{CC} = 5.0\text{V} \pm 5\%$ (9)

Symbol	Parameter	iPLD910-12			iPLD910-15			iPLD910-25			Non-(10) Turbo Mode	Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
$f_{CNT1}^{(13)}$	Max. Counter Frequency $1/(t_{SU} + t_{CO})$ —Ext. Feedback	62.5	75		50	66		33	40			MHz
$f_{CNT2}^{(13)}$	Max. Counter Frequency $1/(t_{CNT})$ —Internal Feedback	76.9	85		66.6	75		40	50			MHz
f_{MAX}	Max. Frequency (Pipelined) $1/(t_{CW})$ —No Feedback	100	110		83.3	100		50	66			MHz
t_{SU}	Input or I/O Setup Time to CLK	8			11			16			+ 40	ns
t_H	Input or I/O Hold Time from CLK	0			0			0				ns
$t_{CO1}^{(13)}$	CLK High to Output Valid			8			9			14		ns
t_{CO2}	CLK High to Output Valid Fed Through Comb. Macrocell			17			20			30	+ 40	ns
$t_{CNT}^{(13)}$	Macrocell Output Feedback to Macrocell Input—Internal Path			13			15			25	+ 40	ns
t_{CL}	CLK Low Time	4			5			8				ns
t_{CH}	CLK High Time	4			5			8				ns
t_{CP}	CLK Period	10			12			20				ns

NOTE:

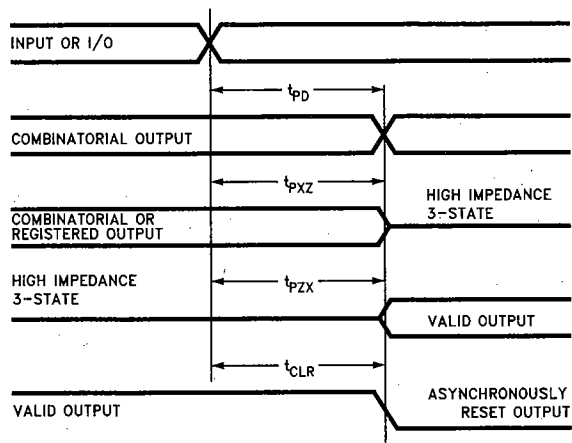
13. Measured with device configured as 24-bit counter.

REGISTER MODE—ASYNCHRONOUS CLOCK A.C. CHARACTERISTICS

$T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$ (9)

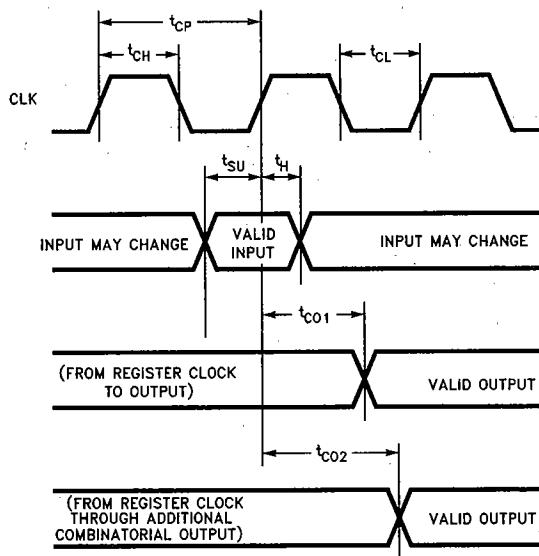
Symbol	Parameter	iPLD910-12			iPLD910-15			iPLD910-25			Non-(10) Turbo Mode	Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
$f_{ACNT1}^{(13)}$	Max. Counter Frequency $1/(t_{ASU} + t_{ACO})$ — Ext. Feedback	52.6	70		45.4	60		27.7	40			MHz
$f_{ACNT2}^{(13)}$	Max. Counter Frequency $1/t_{ACNT}$ — Internal Feedback	76.9	85		66.6	80		40	50			MHz
f_{AMAX}	Max. Frequency (Pipelined) $1/t_{ACW}$ —No Feedback	83.3	90		66.6	80		40	50			MHz
t_{ASU}	Input or I/O Setup to Asynch. CLK	3			4			8			+ 40	ns
t_{AH}	Input or I/O Hold from Asynch. CLK	6			7			8				ns
t_{ACO1}	Asynch. CLK High to Output Valid			16			18			28	+ 40	ns
t_{ACO2}	Asynch. CLK High to Output Valid Fed Through Comb. Macrocell			26			29			44	+ 40	ns
$t_{ACNT}^{(13)}$	Macrocell Output Feedback to Macrocell Input— Internal Path			13			15			25	+ 40	ns
t_{ACL}	Asynch. CLK Low Time	5			6			10				ns
t_{ACH}	Asynch. CLK High Time	5			6			10				ns
t_{ACP}	Asynch. CLK Period	12			15			25				ns

COMBINATORIAL MODE



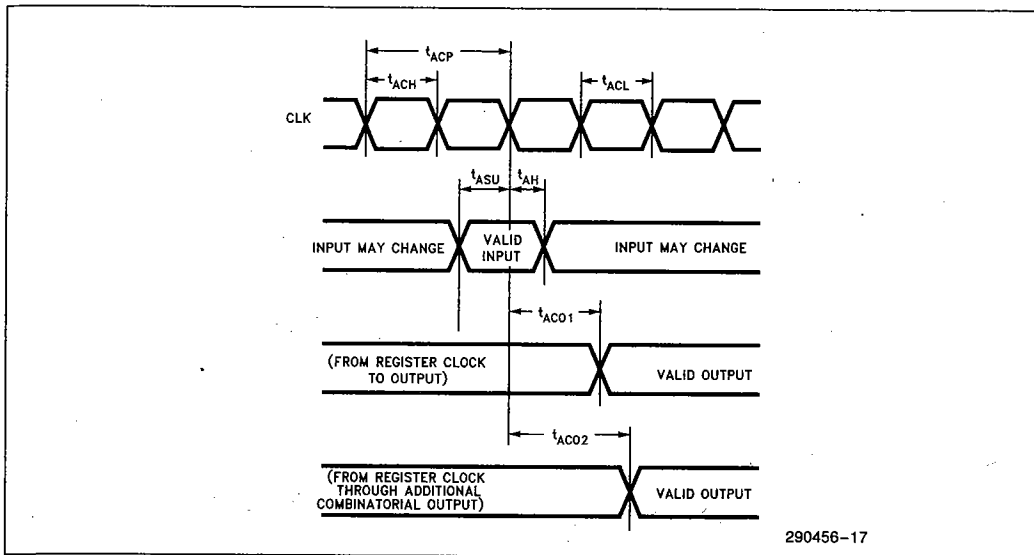
290456-15

SYNCHRONOUS REGISTERED MODE

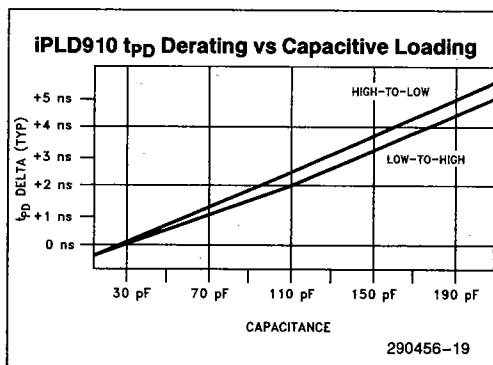
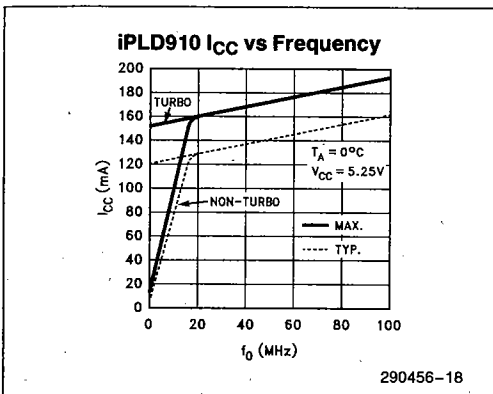


290456-16

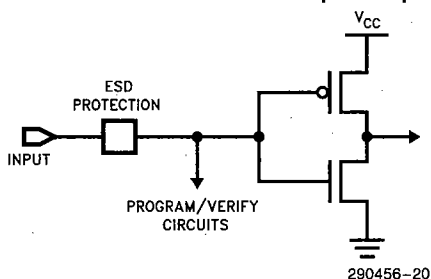
ASYNCHRONOUS REGISTERED MODE



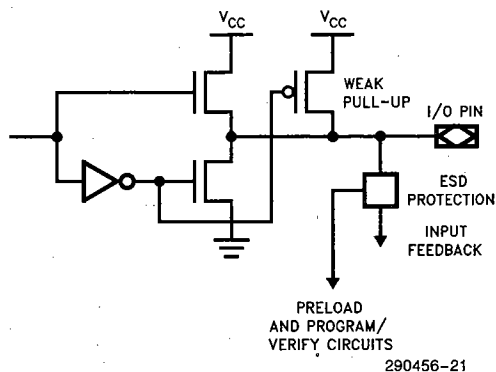
2



Input/Output Equivalent Schematics

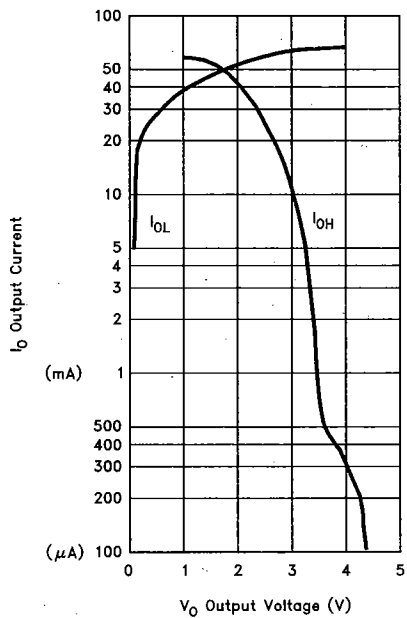


290456-20



290456-21

iPLD910 Output Current in Relation to Voltage



290456-22

CONDITIONS:

$T_A = +70^\circ C$

$V_{CC} = 4.75V$

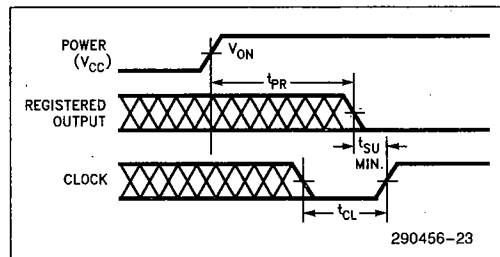
Power-Up Reset

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered-up. Because V_{CC} rise can vary significantly from one application to another, V_{CC} rise must be monotonic.

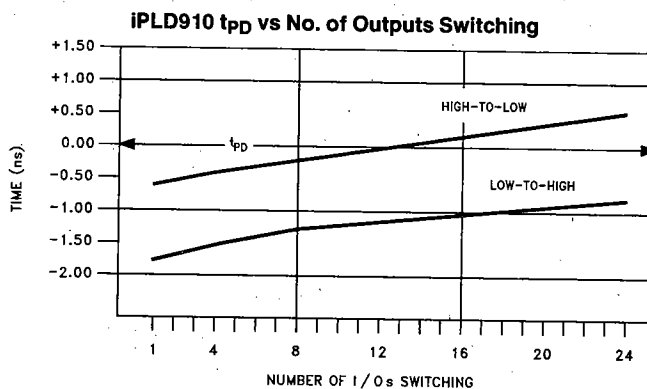
POWER-UP RESET CHARACTERISTICS

Symbol	Parameter	Value
t_{PR}	Power-Up Reset Time	1000 ns Max.
V_{ON}	Turn-On Voltage	4.75V

POWER-UP RESET



290456-23



CONDITIONS:
 $T_A = 70^\circ\text{C}$, $V_{CC} = 4.75\text{V}$, Spec. Load

290456-24

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PACKAGE/TECHNOLOGY SPECIFICATIONS

Description	Specification
θ_{JA} —Junction-to-Ambient Thermal Resistance	44.5°C/W-CerDIP 51°C/W-PDIP 55°C/W-PLCC
θ_{JC} —Junction-to-Case Thermal Resistance	17°C/W-CerDIP 29°C/W-PDIP 16°C/W-PLCC
I_{CC} Hot—Ambient @70°C	125 mA
I_{CC} Typical—Ambient @25°C	125 mA
Process	CHMOS IIIIE, PX 29.5